

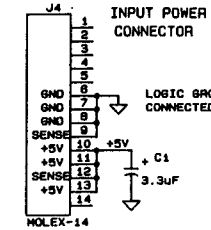
REVISED		EFF	APPROVAL / DATE
LTR	DESCRIPTION	CHK	PROG. ENGR / MFG ENGR
C	RELEASED TO PRODUCTION		
D	INC CDO NO. 28853: ADDED R74		
E	D00 36228: ADDED Z2		
F	D00 40534: U17D WAS SPARE. U17 PIN 13 WAS N/C. U6 PIN 1 WAS +5V.		

SIGNAL NAME	SOURCE/DESTINATION
ALATCH	103 1C8 288
CLK	106 1C8 186 2C8
HLDA	107 186
IA00	104 288 388
IBHE	108 288 388 3A8
IC00/INTA-	105 1C4
IN/10	105 1C4
INTA	105 103
INTR	103 1C8 186
INTRDY-	103 1C8
I/OINT-	1A2 104

SIGNAL NAME	SOURCE/DESTINATION
RAM0-	1C3 1A4
RAM1-	1C3 1A5
ROMORDY-	1A4 1C8
ROM1RDY-	1A5 1C8
SPARE1-	1C3 1D8
SPARE2-	1C3 1D8
TIMER-	1A2 1D4
VIDSLT-	1C3 1C8
VRAM-	1C3 388
VRAMRDY-	3A5 1C8
WRITE	105 288
WRITE	31 9309MHZ
WRITE	3C3 385
WRITE	3C3 107

SIGNAL NAME	SOURCE/DESTINATION
READY-83	87 M/10
CLK-31	5 90-
RESET-29	4 S1-
BUSY-84	88 C/I
ERROR-53	7 A23
PEACK-6	8 A22
LOCK-68	10 A21
NMI-59	11 A20
INTR-57	12 A19
HLDA-85	13 A18
HOLD-84	14 A17
+5V-62	15 A16
D15-51	16 A15
D14-48	17 A14
D13-47	18 A13
D12-46	19 A12
D11-45	20 A11
D10-41	21 A10
D09-39	22 A09
D08-37	23 A08
D07-50	24 A07
D06-48	25 A06
D05-44	26 A05
D04-42	27 A04
D03-40	28 A03
D02-38	29 A02
D01-38	30 A01
D00-38	31 A00
DIR	1 DIR
DIR	11 DIR
DIR	19 DIR
DIR	27 DIR
Vpp	1 Vpp
CE	22 CE
OE	22 OE

TEST CONNECTOR IS WIRED IN PARALLEL WITH U14, EXCEPT THE HOLD LINE, WHICH TRISTATES THE MICROPROCESSOR DURING TESTING.



CAUTION
SUBJECT TO DAMAGE BY
STATIC ELECTRICITY

BASIC DWG NO	DRAWING NO	PART NO

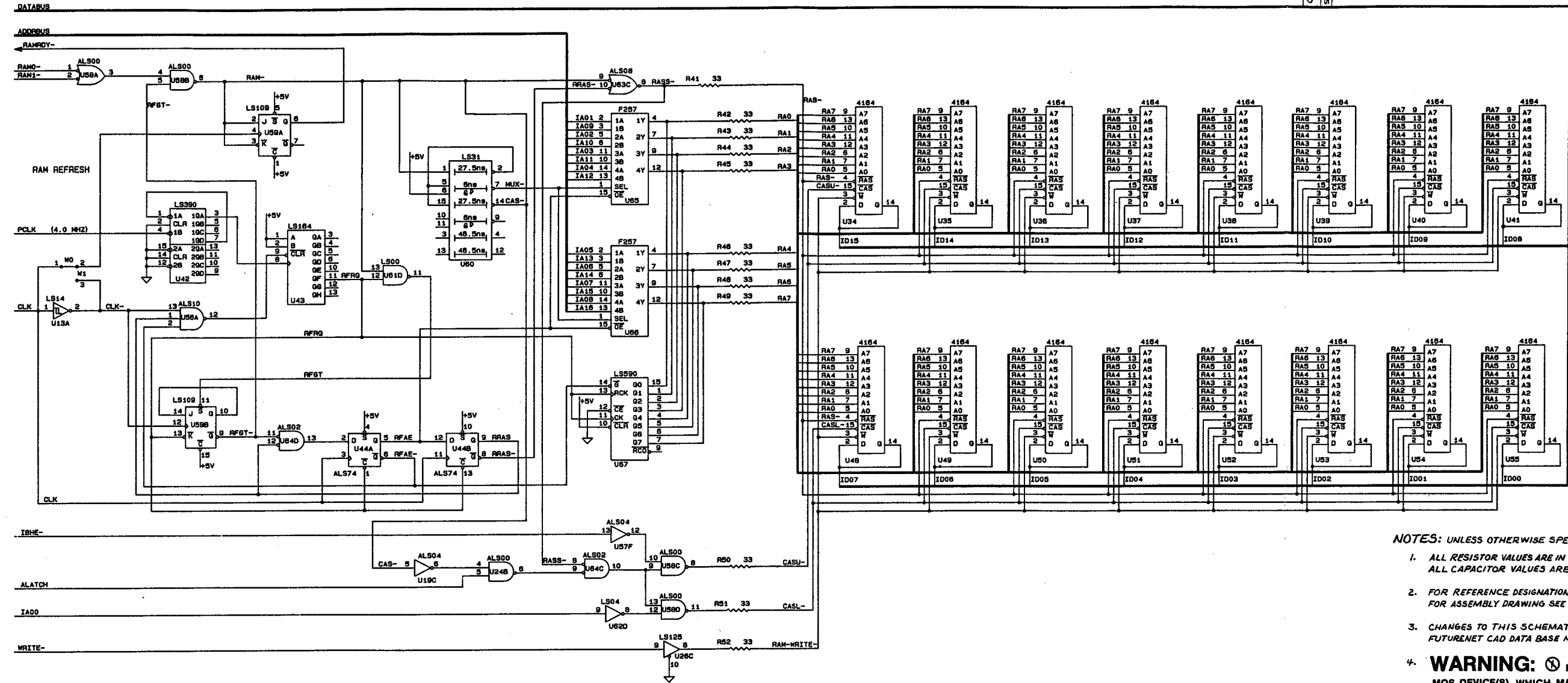
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89536	DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED
TOLERANCE	DIMENSIONS IN INCHES	FINISH
ANGLES		

QTY	ITEM	PART NO	DRAWING NO	DESCRIPTION	REF ID

SCHEMATIC - DEMO/TRAINER
PART NO: D9000A-1080
SCALE: 1 OF 3
REV: F

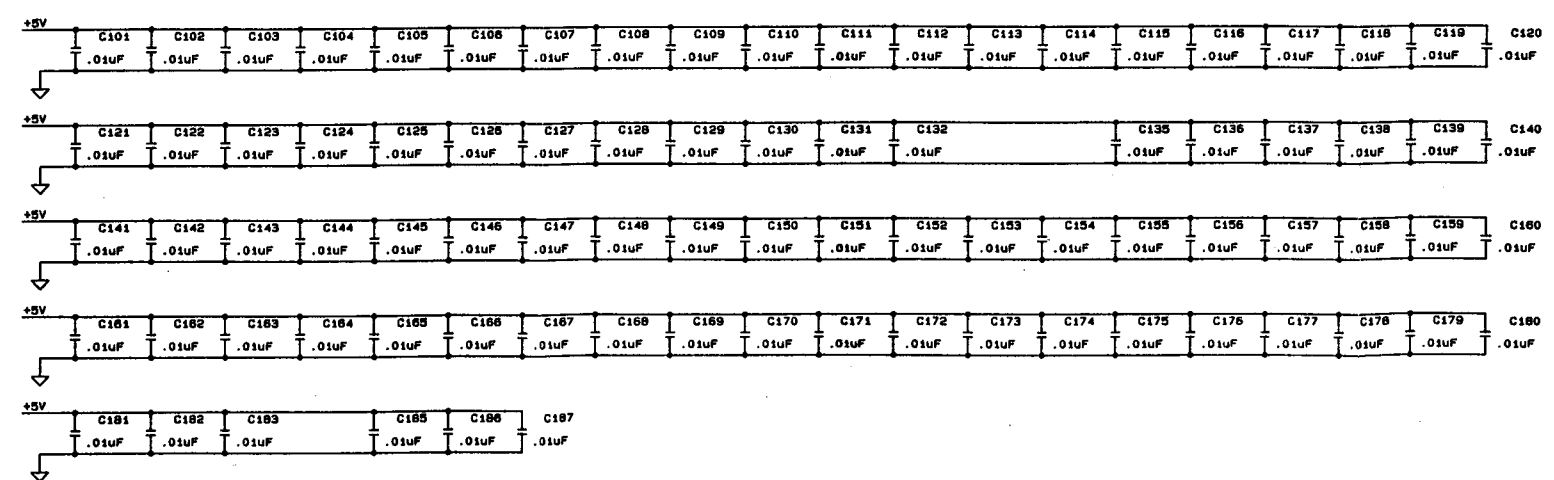
9000A-1080
SH 2 OF 3 REV F

REVISIONS
SEE SHEET 1 FOR REVISIONS



- NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, 5%, ALL CAPACITOR VALUES ARE IN MICROFARADS.
 2. FOR REFERENCE DESIGNATION DRAWING SEE 9000A-1680. FOR ASSEMBLY DRAWING SEE 9000A-1080.
 3. CHANGES TO THIS SCHEMATIC MUST BE MADE THRU FUTURENET CAD DATA BASE NO. 9000A-1080: FD.
 4. **WARNING:** ⚡ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 19.1

BYPASS CAPACITORS



SIGNAL NAME	SOURCE/DESTINATION	SIGNAL NAME	SOURCE/DESTINATION
ALATCH	103 1C8 2B8	ROM0-	1C3 1A4
CLK	106 1C8 1B8 2C8	ROM1-	1C3 1A5
H0A	1C7 1B8	ROMRDY-	1A4 1C8
IA00	1C4 2B8 3B8	ROMRDY-	1A5 1C8
IBHE-	1D5 2B8 3B8 3A8	SPARE1-	1C3 1D8
IC00/INTA-	1D5 1C4	SPARE2-	1C3 1D9
IN/10	1D5 1C4	TIMER-	1A2 1D4
INTA	1D5 1D3	VIDSLT-	1C3 1C8
INTR	1D3 1C8 1B8	VRAM-	1C3 3B8
INTRDY-	1D3 1C8	VRAMRDY-	3A5 1C8
I/OINT-	1A2 1D4	WRITE-	1D5 2B8
		31.9399MHZ	3C3 3B5
		18MHZ	3C3 1D7

SIGNAL NAME	SOURCE/DESTINATION
I/OISLT-	1C3 1C8 1A3
IPOLL-	1C4 1C4
IREAD-	1D5 1C3 1A3
IWRITE-	1D5 1C3 1A3
PLK	1D5 2C8
PPISLT-	1C3 1C2 1C8
RAM0-	1C3 2D8
RAM1-	1C3 2D8
RAMRDY-	2D8 1C8
READ-	1D5 1D4 1A5 1A4 3B8
READY-	1D5 1D5 1C8 1B8
RESET	1D5 1C5 1C2 1B5 1A3 3A8

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STATIC ELECTRICITY

FLUKE	JOHN FLUKE MFG CO. INC P O BOX C9090 EVERETT WA 98206
89536	DO NOT SCALE DRAWING
SCHEMATIC — DEMO/TRAINER	
PART NO	SIZE DPA4-N, N0
	D 9000A-1080
SCALE	SH 2 OF 3 REV F